# Nearly Dispersionless Microstrip for 100 GHz Pulses Utilizing a Buried Silicide Groundplane

K.W. Goossen, H. Roskos, M.C. Nuss, D.W. Kisker, B. Tell
AT&T Bell Laboratories, Holmdel, NJ 07733

A.E. White, K.T. Short, D.C. Jacobson and J.M. Poate
AT&T Bell Laboratories, Murray Hill, NJ 07974

*Abstract* - **Measurements of pulse propagation on microstrip lines on silicon that use a buried highly conducting $CoSi_2$ groundplane are presented. These lines show significant reductions in dispersion compared to lines using a standard groundplane on the back of the substrate, due to the much smaller conductor separation. Rise times of 100 GHz pulses increase only from 2.5 ps to 3.7 ps on the buried groundplane microstrip after 5 mm propation, compared to 2.7 ps to 11.3 ps on a conventional microstrip. The $CoSi_2$ layer is formed by an ion-implant and alloy technique that results in a crystalline silicon overlayer allowing device fabrication.**

## I. Introduction

It is well known that electrical pulses traveling on microstrip transmission lines propagate in a quasi-TEM mode, and that this mode suffers dispersion near the TE cutoff frequency.[1] This dispersion is caused by a change in the field pattern of the quasi-TEM mode. In its DC configuration, the field lines are distributed in air and in the substrate in comparable percentages, while at frequencies higher than the TE cutoff, the field lines are all in the substrate. Therefore the effective index changes from a weighted average of the indices of air and the substrate at DC, to that of the substrate at high frequencies (Fig. 1). (The significance of the TE cutoff frequency is somewhat coincidental in microstrip. Actually the quasi-TEM mode changes its field pattern in response to the conductor separation (h) becoming comparable to the wavelength of the radiation. Since h equals the substrate thickness in conventional microstrip, and the TE mode is a slab mode traveling in the substrate, the TE cutoff also occurs when h becomes comparable to the wavelength.)

The TE cutoff frequency is given by $f_{TE}=c/[4h(\varepsilon_r-1)]^{1/2}$. Therefore as h is reduced, the onset of dispersion is pushed to higher frequencies. For typical microwave integrated circuits, $h=500$ μm, which yields $f_{TE}=46$ GHz for silicon substrates, and slightly lower for GaAs. Therefore, pulses with rise times of a few picoseconds will markedly disperse. We show below that a pulse with a 2.7 ps rise time broadens to 11.3 ps after propagating 5 mm. However, if h were reduced to 10 μm, $f_{TE}$ would increase to 2.3 THz, dramatically reducing dispersion.[2]

We have developed a microstrip transmission line on silicon with a buried silicide groundplane,[3] so that h is reduced to roughly 10 μm without having to thin the substrate, which would result in breakage and complicate device processing. We show below that a 2.5 ps pulse traveling along this microstrip broadens to only 3.7 ps after 5 mm, a significant reduction in dispersion compared to standard microstrip. The technique for producing the silicide layer results in a crystalline overlayer of silicon, which can support device fabrication. Therefore these results should significantly impact the microwave monolithic integrated circuit technology.

## II. Theory

Dispersion in a transmission line is caused by a change of the guide phase velocity ($v_p=c/n_{eff}$) with frequency (f). Since an electrical pulses is broadband, it becomes distorted as it propagates. The effective index at DC ($n_{eff0}$), as mentioned, has a value between than of the substrate ($n_r$) and air (1). It may be found by a conformal mapping analysis of the static field pattern induced by applying a bias between the conductors. This has been performed by Schneider [4] to obtain

$$n_{eff0}^2=\frac{1}{2}\left[(\varepsilon_r+1)+\frac{\varepsilon_r-1}{(1+10h/w)^{1/2}}\right] \quad . \qquad (1)$$

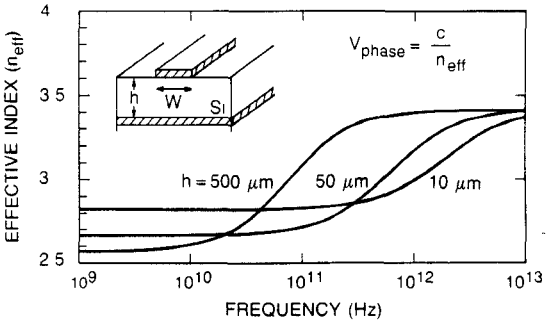


Fig. 1: Effective index of microstrip vs. frequency for w=10 μm. As conductors are brought closer, dispersion is pushed to higher frequencies.



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Here w is the width of the center conductor. As shown in Fig. 1 $n_{eff0}$ becomes closer to $n_r$ as h/w becomes smaller. This is logical since there is less fringing into the air. Note that a side benefit of the buried groundplane configuration is reduced fringing and hence less crosstalk.

At higher frequencies the field distribution changes, and as stated, eventually all the lines are in the substrate. This has been quantified in Ref. 1, where a full-wave analysis was performed and curve-fitted to obtain

$$n_{eff} = n_{eff0} + \frac{n_r - n_{eff0}}{1+4F^{-1.5}} \quad , \tag{2}$$

where $F=(f/f_{TE})[0.5+(1+2\log(1+w/h))]$. In Fig. 1 the effective index is plotted vs. frequency for w=10 μm and h=500, 50, and 10 μm. The change of $n_{eff}$ with frequency is evident, as is the fact that as h becomes smaller the freqencies about which the maximum dispersion occurs become much higher.

The physical reason for the dependence of the dispersive frequencies on the conductor separation may be thought of as follows: In order to set up a static distribution one conductor must be able to sense the charge distribution on the other conductor in a time short compared to the cycle period. Since this "sensing" occurs at the speed of light the time it takes to propagate between the conductors must be short compared to 1/f. Therefore as the conductor spacing is made smaller a static distribution may be maintained to much higher frequencies.

From Fig. 1, the frequency of maximum dispersion is 70 GHz for h=500 μm and 2.5 THz for h=10 μm. Therefore since Si wafers are typically 500 μm thick we would expect large dispersion for 100 GHz pulses on standard microstrip; negligible dispersion should occur on buried-groundplane microstrip. This is shown in Fig. 2 where the effect of propagating a logic pulse 2 mm for both cases is shown (see Ref. 2). For the standard case there is large distortion while for the buried-groundplane case there is negligible distortion.

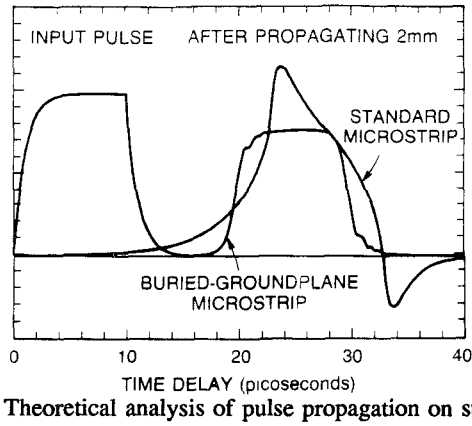


Fig. 2: Theoretical analysis of pulse propagation on standard and buried groundplane microstrip, showing much greater distortion for the standard case.

## III. Fabrication

The silicide layer (e.g. $CoSi_2$) is produced by implanting metal ions (e.g., cobalt) into silicon and subsequently annealing at high temperature. This results in a planar crystalline silicide layer with sharp interfaces with an overlayer of crystalline silicon, hence the name for the technique, mesotaxy.[3] In our case the $CoSi_2$ layer is 3000 Å thick and has a resistivity of 10 μΩcm, only a few times higher than bulk Al and comparable to evaporated Al. We used a (100) n-type (8 Ωcm) substrate that was implanted with Co ions of 1.5 MeV energy at a dose of $8.5\times10^{17}$ $cm^{-2}$. Then the sample was annealed at 600°C for 1 hour, 1000°C for 45 min. and finally at 1100°C for 1.5 hour. This resulted in a 9000 Å thick silicon overlayer. Since the silicide is formed at such high temperatures it is stable to subsequent device processing.[5] A 7 μm thick epilayer of nominally undoped silicon was then grown on top of the wafer by chemical vapor deposition (CVD). Atop this a 3000 Å CVD $SiO_2$ film was deposited for DC isolation. A 2700 Å thick aluminum center conductor was subsequently deposited by thermal evaporation and patterned to a width of 5 μm.

## IV. Measurement Technique

The measurements were performed using picosecond optoelectronic techniques.[6] Two short lengths of microstrip (sampling lines) were patterned perpendicular to the center conductor with a 5 μm gap separating them from the center conductor. These sampling lines are separated by the desired propagation distance to be measured. Over these gaps a 4000 Å thick polycrystalline CdTe film was deposited by UV-enhanced MOCVD. This material is photoconductive with a subpicosecond photocurrent decay time.[7] One sampling line is biased with respect to the main line. A colliding-pulse-modelocked Rhodamine 6G dye laser is used to deliver a sequence of 100 fs optical pulses onto this gap, thus producing picosecond electrical pulses on the main line. A second sequence of identical pulses, but delayed from the first, is focussed onto the second gap, which is unbiased. By measuring the photocurrent on this sampling gate at a fixed delay, the strength of the propagated electrical pulse at that time delay is found. By varying the delay, the propagated electrical pulse is mapped in the time domain.

## V. Results

For comparison, we also fabricated microstrip lines with conventional groundplanes on 500 μm thick Si substrates. Note that these conventional lines are on highly resistive (500 Ωcm) silicon wafers. Therefore they should have negligible substrate losses. In Fig. 3 we

show the generated electrical pulse on this standard microstrip after propagating 0.1, 2, and 5 mm. The time scale of each plot has been shifted and the amplitude normalized so that the pulses are atop each other. As stated, the rise time, initially 2.7 ps, increases significantly, to 11.3 ps after 5 mm propagation. There is also significant ringing in the trailing part of the pulses. The amplitudes of the pulses are 1, 0.32 and 0.085 for the respective propagation distances. Both dispersion and losses contribute to this reduction.

In contrast, we show in Fig. 4 pulse propagation data for the buried-groundplane microstrip. As a side benefit it appears that a shorter pulse can be *generated* on the buried-groundplane microstrip than on a standard microstrip (after 0.1 mm propagation effects should be negligible in either.) The pulse shows little dispersion, with the rise-time increasing from 2.5 ps at 0.1 mm to only 3.7 ps after 5 mm. The trailing part of the pulse shows no ringing, although there appears to be a rise in the trailing pedestal. The amplitude of the pulse is 1, 0.31 and 0.062 for the respective distances. Therefore the "rise" of the trailing pedestal is an artifact of the normalization- actually it remains constant while the main peak gets smaller. We believe this pedestal is due to residual conductivity in the CdTe photoconductor.

Figure 5 shows the rise time of the pulses as a function of distance for the standard and buried-groundplane configuration. The rise-time of the standard microstrip increases nearly linearly with propagation distance. Only a slight increase is seen for the buried-groundplane microstrip.

The losses on the buried-groundplane microstrip are somewhat higher than in the standard case. To determine the source of these losses we repeated the measurements at lower temperatures. Fig. 6 shows the pulse on buried-groundplane microstrip after propagating 0.1 and 5 mm at 10 K. The risetime of the pulse at 0.1 mm is 2.5 ps and its FWHM is 1.6 ps. To our knowledge, this is the shortest electrical pulse ever generated on a microstrip line. No pedestal is observed in the trailing part indicating that there is no residual conductivity in the CdTe at 10 K. After 5 mm propagation the pulse amplitude is reduced to 0.35 of the input- the losses have reduced considerably. The distortion of the pulse has also reduced slightly. A negative lobe does occur in the trailing part of the pulse. Such a lobe qualitatively should appear due to dispersion, but not to this magnitude. For the lossless case on microstrip, it is trivial to show that gaussian pulses will propagate as

$$v(z,t)=\mathrm{Re}\left[\frac{1+\mathrm{erf}\left(\frac{it_d/\tau}{1+i\tau_B^2/\tau^2}\right)}{(1+i\tau_B^2/\tau^2)^{1/2}}\exp\left[\frac{t_d^2/\tau^2}{1+i\tau_B^2/\tau^2}\right]\right]$$

where $\tau_B^2=z(n_r-n_{eff0})/(\pi c f_i)$, $t_d=t-n_{eff0}z/c$, and

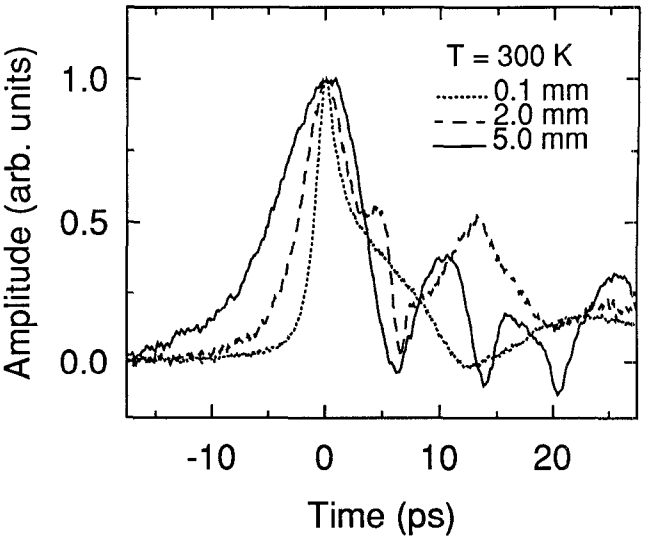


Fig. 3: Experimental propagation on standard microstip. The time delay and amplitudes have been normalized so the curves lie atop each other.

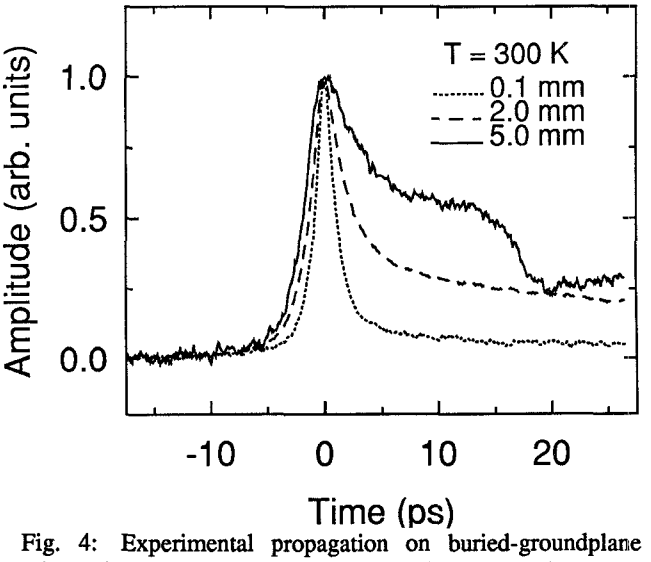


Fig. 4: Experimental propagation on buried-groundplane microstrip, showing much less dispersion. The plots have been scaled as in Fig. 3.

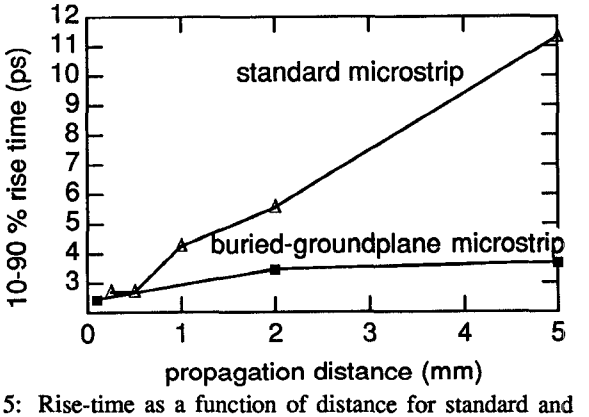


Fig. 5: Rise-time as a function of distance for standard and buiried-groundplane microstrip.

$f_i = f/F$. From this a negative lobe in the trailing edge should appear.

At further time delay the reflection of the pulse from the contact pad can be seen in the 5 mm curve. The distance from the 5 mm sampling gate and the contact pad is 1 mm, so the reflection has traveled 2 mm further than the 5 mm pulse. This reflection provides an additional confirmation of the reduction of losses since it is 0.7 of the 5 mm pulse. (The contact pad should reflect about 0.94 of the pulse.)

By measuring the attenuation of the reflected pulse as a function of temperature we find quite clearly that most of the loss at room temperature is shunt loss in the silicon, and very little is due to either conductor. This is shown in Fig. 7. As the temperature is lowered from 300 to 100 K the loss changes very little, reducing to about 95 % of its value at 300 K. However, the resistivity of our silicide decreases by a factor of five over this temperature range.[8] Therefore we conclude that conductor loss in the silicide (or the Al center conductor, for that matter, since its resistivity also lowers by a factor of five) contributes little to the total loss. However, below 100 K there is a rapid decrease in the loss with temperature. This corresponds to the temperature at which carriers freeze out in silicon, causing its resitivity to increase greatly. Therefore we conclude that most of the loss at room temperature is shunt loss in the silicon. This loss could either be occuring in the epilayer of silicon, or in the overlayer of host substrate above the silicide after the implant, or due to leakage of the field lines beneath the silicide. Recall that our host substrate had only 8 Ωcm resistivity. At the time of this writing we just repeated measurements with 1000 Ωcm host substrates. No change in the room temperature losses was observed, confirming that the epilayer is the source of the losses. We endeavor to obtain purer silicon epilayers.

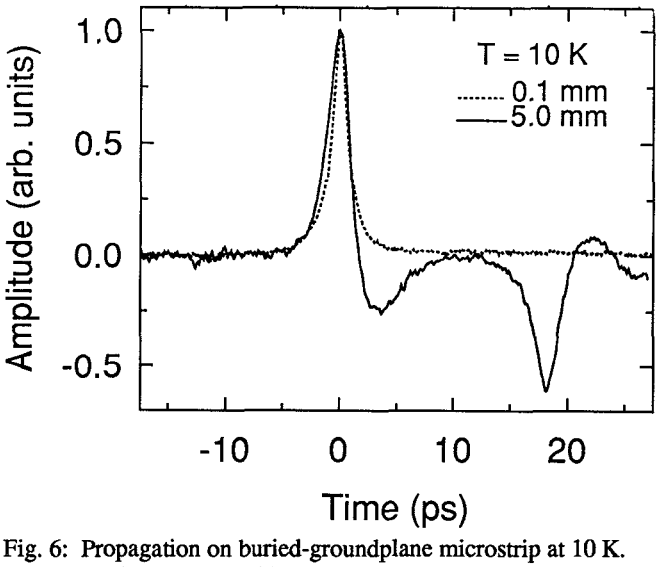


Fig. 6: Propagation on buried-groundplane microstrip at 10 K. Note reflection at 18 ps- this has propagated 2 mm further than main peak.

## VI. Conclusion

We have demonstrated a microstrip configuration using a buried silicide groundplane, which we measure to have significantly less dispersion for picosecond pulses than standard microstrip. Temperature dependent measurements indicate that no loss penalty is incurred by using the silicide as the groundplane. This has significance for future integrated circuits in the 100 GHz range.

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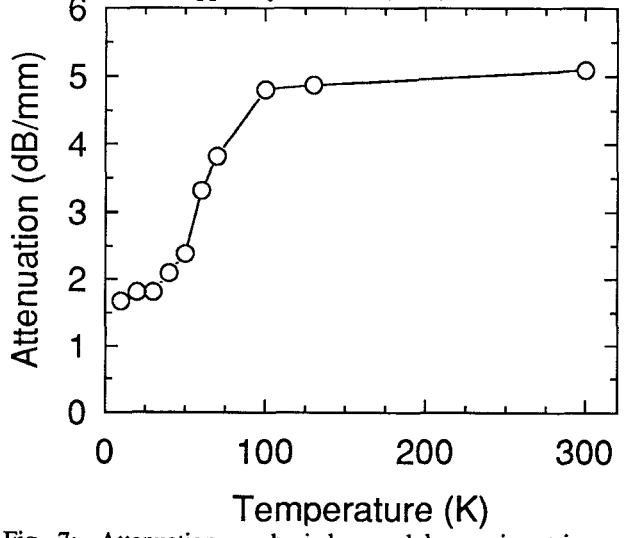


Fig. 7: Attenuation on buried-groundplane microstrip vs. temperature. This indicates most of loss is from substrate and very little from conductors.